IN THE CLAIMS

1. (currently amended) A memory device comprising:

a memory array; and

redundant circuitry connected to the memory array, the redundant circuitry comprising a register adapted to indicate different types of ~~a~~ row-to-row short<u>s</u>.

2. (original) The memory device of claim 1, wherein the redundant circuitry further comprises an address decoder for selecting, during an erase operation, x rows of the memory array for a row-to-row short of x rows when x rows are shorted together and x is even or x + 1 rows for a row-to-row short of x + 1 rows when x rows are shorted together and x is odd.

3. (original) The memory device of claim 1, wherein the redundant circuitry further comprises control circuitry for controlling memory operations and for instructing an address counter, during an erase operation, to increment row addresses of rows of the memory array by x rows for a row-to-row short of x rows when x rows are shorted together and x is even or x + 1 rows for a row-to-row short of x + 1 rows when x rows are shorted together and x is odd.

4. (original) A memory device comprising:

a memory array; and

redundant circuitry connected to the memory array, the redundant circuitry comprising a register adapted to indicate an x-row short when x rows of the memory are shorted together and x is even and an (x+1)-row short when x rows of the memory are shorted together and x is odd.

5. (original) The memory device of claim 4, wherein the redundant circuitry further comprises an address decoder for selecting, during an erase operation, x rows of the memory array when x is even or x + 1 rows when x is odd.

6. (original) The memory device of claim 4, wherein the redundant circuitry further comprises a redundancy circuit for comparing row addresses of the rows of the memory array to a redundancy address of the register.

7. (original) The memory device of claim 4, wherein the memory array comprises non-volatile memory cells.

8. (original) The memory device of claim 4, wherein the redundant circuitry further comprises control circuitry for controlling memory operations and for instructing an address counter, during an erase operation, to increment row addresses of the rows of the memory array by x rows when x is even or x + 1 rows when x is odd.

9. (original) A memory device comprising:

a memory array arranged in rows and columns and having at least four redundant rows for selectively replacing associated defective rows in the memory array;

a register associated with each of the redundant rows, each register adapted to store a redundancy address corresponding to an address of the associated defective row in the memory array and to store a first bit level indicative of an x-row short when x rows of the memory array are shorted together and x is even, or a second bit level indicative of an (x + 1)-row short when x rows of the memory array are shorted together and x is odd;

a redundancy circuit for comparing row addresses of the rows of the memory array to a redundancy address stored in a redundant element's register; and

control circuitry to control memory operations, wherein the control circuitry is adapted to apply a program cycle of an erase operation to x rows of the memory array simultaneously and to instruct an address counter to increment the row addresses by x rows when the first bit level is stored in that redundant element's register and one of the row addresses matches the redundancy address stored in that redundant element's register, and wherein the control circuitry is adapted to apply the

program cycle to x + 1 rows of the memory array simultaneously and to instruct the address counter to increment the row addresses by x + 1 rows when the second bit level is stored in that redundant element's register and one of the row addresses matches the redundancy address stored in that redundant element's register.

10. (original) The memory device of claim 9, further comprising an address decoder for selecting, during an erase operation, when one of the row addresses matches the redundancy address stored in that redundant element's register, x rows of the memory array when the first bit level is stored in that redundant element's register or x + 1 rows when the second bit level is stored in that redundant element's register.

11. (original) The memory device of claim 10, wherein the address decoder is adapted to select, during an erase operation, one row of the memory array when one of the row addresses does not match the redundancy address stored in that redundant element's register.

12. (original) The memory device of claim 9, wherein the control circuitry is further adapted to instruct the address counter, during an erase operation, to increment the row addresses by one row when one of the row addresses does not match the redundancy address stored in that redundant element's register.

13. (original) The memory device of claim 9, wherein the control circuitry is further adapted to apply a program cycle of an erase operation to one row of the memory array when one of the row addresses does not match the redundancy address stored in that redundant element's register.

14. (original) The memory device of claim 9, wherein the memory array comprises non-volatile memory cells.

15. (original) A memory device, comprising:

a memory array having primary elements and redundant elements;

control circuitry for controlling access to the memory array;

redundancy circuitry for selectively routing access requests directed to a defective primary element to an associated redundant element; and

a register associated with each of the redundant elements, each register adapted to store an address representative of a defective primary element and an error code;

wherein the control circuitry is adapted to perform an erase operation on the memory device;

wherein the control circuitry is further adapted to receive the error code from a redundant element's register when an address request for the erase operation matches the address stored in that register; and

wherein the control circuitry is further adapted to disable the redundancy circuitry during a portion of the erase operation if the received error code is indicative of a row-to-row short.

16. (original) The memory device of claim 15, further comprising an address decoder for selecting, during the erase operation, x rows of the memory array when the error code is indicative of a row-to-row short of x rows when x rows are shorted together and x is even or x + 1 rows when the error code is indicative of a row-to-row short of x + 1 rows when x rows are shorted together and x is odd.

17. (original) The memory device of claim 15, wherein the control circuitry is further adapted to instruct an address counter, during the erase operation, to increment row addresses of the rows of the memory array by x rows when the error code is indicative of a row-to-row short of x rows when x rows are shorted together and x is even or x + 1 rows when the error code is indicative of a row-to-row short of x + 1 rows when x rows are shorted together and x is odd.

18. (original) A method for operating a memory device, the method comprising:

reading a bit of a redundant register, the bit being at a first level indicative of an x-row short when x rows of a memory array are shorted together and x is even or a second level indicative of an (x + 1)-row short when x rows of the memory array are shorted together and x is odd;

applying a program cycle of an erase operation to the x rows shorted together when the bit is at the first level or to the x rows shorted together plus a next row when the bit is at the second level; and

incrementing a row address by x rows when the bit is at the first level or by x + 1 rows when the bit is at the second level.

19. (original) The method of claim 18, further comprising matching a row address of a row of the memory array with a redundancy address of the redundant register before reading the bit of the redundant register.

20. (original) The method of claim 18, wherein applying the program cycle of the erase operation comprises applying a pre-program or a soft program cycle of the erase operation.

21. (original) A method for operating a memory device, the method comprising:

comparing a row address of a row of a memory array to a redundancy address of a register, the redundancy address corresponding to a defective row of the memory array;

reading a bit of the register when the row address matches the redundancy address, the bit being at a first level indicative of an x-row short when x rows of the memory array are shorted together and x is even or a second level indicative of an (x + 1)-row short when x rows of the memory array are shorted together and x is odd;

applying a program cycle of an erase operation to the x rows shorted together simultaneously when the bit is at the first level or to the x rows shorted together plus a next row simultaneously when the bit is at the second level; and

incrementing the row address by x rows when the bit is at the first level or by x + 1 rows when the bit is at the second level.

22. (original) The method of claim 21, wherein applying the program cycle of the erase operation comprises applying a pre-program or a soft program cycle of the erase operation.

23. (original) The method of claim 21, further comprising applying the program cycle to one row when the row address does not match the redundancy address.

24. (original) The method of claim 21, further comprising incrementing the row address by one row when the row address does not match the redundancy address.

25. (original) A method of operating a memory device, comprising:

comparing an address request to an address stored in a register, wherein the address stored in the register is representative of a defective row or column;

when the address request matches the address stored in the register, relaying an error code associated with the address stored in the register to a control circuitry adapted to perform at least erase operations on the memory device;

if the error code is indicative of a row-to-row short, disabling redundant circuitry during a portion of the erase operation; and

if the error code is indicative of an isolated error, performing a typical erase operation using the redundant circuitry.

26. (original) The method of claim 25, wherein the method, after performing an erase operation, further comprises:

incrementing an address counter by one if the address request does not match the address stored in the register or the address request matches the address stored in the register and the error code is indicative of an isolated error;

incrementing the address counter by x if the address request matches the address stored in the register and the error code is indicative of a row-to-row short of x rows when x rows are shorted together and x is even; and

incrementing the address counter by x +1 if the address request matches the address stored in the register and the error code is indicative of a row-to-row short of x + 1 rows when x rows are shorted together and x is odd.

27. (original) The method of claim 25, further comprising when the address request matches the address stored in the register, performing the at least erase operations on x rows when the error code is indicative of a row-to-row short of x rows when x rows are shorted together and x is even or x + 1 rows when the error code is indicative of a row-to-row short of x + 1 rows when x rows are shorted together and x is odd.

28. (original) A flash memory device comprising:

a memory array comprising non-volatile cells; and

redundant circuitry connected to the memory array, the redundant circuitry comprising a register adapted to indicate an x-row short when x rows of the memory are shorted together and x is even and an (x+1)-row short when x rows of the memory are shorted together and x is odd.

29. (original) The flash memory device of claim 28, wherein the redundant circuitry further comprises an address decoder for selecting, during an erase operation, x rows of the memory array when x is even or x + 1 rows when x is odd.

30. (original) The flash memory device of claim 28, wherein the redundant circuitry further comprises a redundancy circuit for comparing the row addresses of the rows of the memory array to a redundancy address of the register.

31. (canceled)

32. (original) The flash memory device of claim 28, wherein the redundant circuitry further comprises control circuitry for controlling memory operations and for instructing an address counter, during an erase operation, to increment row addresses of the rows of the memory array by x rows when x is even or x + 1 rows when x is odd.

33. (original) A flash memory device comprising:

a memory array of non-volatile memory cells arranged in rows and columns and having at least four redundant rows for selectively replacing an associated defective row in the memory array;

a register associated with each of the redundant rows, each register adapted to store a redundancy address corresponding to an address of the associated defective row in the memory array and to store a first bit level indicative of an x-row short when x rows of the memory array are shorted together and x is even, or a second bit level indicative of an (x + 1)-row short when x rows of the memory array are shorted together and x is odd;

a redundancy circuit for comparing row addresses of the rows of the memory array to a redundancy address stored in a redundant element's register; and

control circuitry to control memory operations, wherein the control circuitry is adapted to apply a program cycle of an erase operation to x rows of the memory array simultaneously and to instruct an address counter to increment the row addresses by x rows when the first bit level is stored in that redundant element's register and one of the row addresses matches the redundancy address stored in that redundant element's register, and wherein the control circuitry is adapted to apply the program cycle to x + 1 rows of the memory array simultaneously and to instruct the address counter to increment the row addresses by x + 1 rows when the second bit level is stored in that redundant element's register and one of the row addresses matches the redundancy address stored in that redundant element's register.

34. (original) The flash memory device of claim 33, further comprising an address decoder for selecting, during an erase operation, when one of the row addresses matches the redundancy address stored in that redundant element's register, x rows of the memory array when the first bit level is stored in that redundant element's register or x + 1 rows when the second bit level is stored in that redundant element's register.

35. (original) The flash memory device of claim 34, wherein the address decoder is adapted to select, during an erase operation, one row of the memory array when one of the row addresses does not match the redundancy address.

36. (original) The flash memory device of claim 33, wherein the control circuitry is further adapted to instruct the address counter, during an erase operation, to increment the row addresses by one row when one of the row addresses does not match the redundancy address stored in that redundant element's register.

37. (original) The flash memory device of claim 33, wherein the control circuitry is further adapted to apply a program cycle of an erase operation to one row of the memory array when one of the row addresses does not match the redundancy address stored in that redundant element's register.